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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,555	09/30/2003	Frank Yauchee Hui	Hui 6/075903-235	6518

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BEUSSE BROWNLEE WOLTER MORA & MAIRE, P. A.
390 NORTH ORANGE AVENUE
SUITE 2500
ORLANDO, FL 32801

EXAMINER	
MAGEE, THOMAS J	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 11/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,555	HUI, FRANK YAUCHEE	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 01302004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections – 35 U.S.C. 102

1.The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Or

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 3, 5, 13 – 15, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Iyer et al. (US 6,433,404 B1).

3. Regarding Claim 1, Iyer et al. disclose a fusible link device disposed on a semiconductor substrate (101) (Figure 5) comprising:

a first material (112) having a first resistance,

a second material (114) having a second resistance overlying the first material layer (14), wherein the second sheet resistance is less than the first sheet resistance (Col. 4, lines 45 – 46),

wherein the fusible link is programmable to an opened state in which an opening is formed

in the first and second material layers (Col. 3, lines 53 – 64), and

wherein in a closed state the first and second material layers provide a current path therethrough (Col. 3, lines 47 – 53).

4. Regarding Claim 2, Iyer et al. disclose (Col. 5, lines 4 – 15) a fusible link wherein a material of the first material layer comprises doped polysilicon (Col. 4, lines 8 – 12; 23 – 32).

5. Regarding Claim 3, Iyer et al. disclose (Col. 4, lines 19 – 20) a fusible link, wherein a material of the second material layer (114) comprises a metal silicide.

6. Regarding Claim 5, Iyer et al. disclose that current is supplied (from a current source) for controllably passing a current through the doped polysilicon layer and silicide layer for creating openings therein (Col. 3, lines 53 – 64).

7. Regarding Claim 13, Iyer et al. disclose a method for forming a fusible link in a semiconductor integrated circuit, comprising:

providing a substrate (101) (Figure 5),

forming a first material (112) overlying the substrate, having a first resistance,

forming a fusible link region (106) from the first material layer,

forming a second material (114) overlying the first material layer, having a second resistance overlying the first material layer (14), wherein the second sheet resistance is less than the first sheet resistance, and

forming an opening in the first and second material layers (Col. 3, lines 53 – 64) to program the fusible link to an open state.

8. Regarding Claim 14, Iyer et al. disclose that the step of forming the first material layer comprises forming a doped polysilicon layer (Col. 4, lines 8 – 12; 23 – 32).

9. Regarding Claim 15, Iyer et al. disclose that the step of forming the second material layer (114) comprises forming a metal silicide layer (Col. 4, lines 19 – 20).

10. Regarding Claim 17, Iyer et al. disclose that the step of forming an opening comprises pass-
ing a current through the doped polysilicon layer and the silicide layer for creating openings therein (Col. 3, lines 53 – 64).

11. Claims 9 – 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al. (US 6,703,263 B2).

12. Regarding Claim 9, Wang et al. disclose a semiconductor integrated circuit comprising:

a substrate (101) (Figure 5),

doped regions (6) within the substrate, wherein the doped regions form active devices (Col. 5, lines 50 – 54),

a fuse structure (200) comprising:

a first material layer (24) (Col. 6, lines 5 – 8) having a first sheet resistance,

a second material layer (26) (Col. 6, lines 36 – 39) having a second sheet resistance, wherein the second sheet resistance is less than the first sheet resistance.

wherein the fuse structure is programmable to an opened state in which an opening is formed in the first and second material layers (Col. 2, line 63 through Col.3, line 6).

wherein a closed state, and

wherein in a closed state the first and second material layers are intact (Col. 1, lines 54 – 57).

13. Regarding Claim 10, Wang et al. disclose that a MOSFET active device is formed from doped regions (6) (Figure 5) within the substrate, wherein the MOSFET further comprises a gate, wherein a material (24) (tungsten nitride) (Figure 5) of the gate comprises the first material layer (24).

14. Regarding Claim 11, Wang et al. disclose isolation regions (10) between active devices, wherein the fuse structure (200) (Figure 5) is disposed over an isolation region.

15. Regarding Claim 12, Wang et al. disclose that the material of the isolation region comprises silicon dioxide (Col. 4, lines 52 – 55).

Claim Rejections – 35 U.S.C. 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 6, 7, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iyer et al.,as applied to Claims 1 – 3, 5, 13 – 15, and 17.

18. Regarding Claims 6 and 18, Iyer et al. do not disclose current and voltage levels used for the fusible link during creation of openings. However, parameters such as voltage level and current level are subject to routine experimentation and optimization to achieve the desired fuse element "openings" with a minimum of stray leakage and/or damage to structure. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the values of current and voltage as claimed to attain a "blown" fuse with minimal damage to underlying or adjacent structure.

19. Regarding Claim 7, Iyer et al. discloses the application of a voltage (bias) across the fuse structure (Col. 3, lines 53 – 64). Iyer et al. do not disclose the presence of a controllable switch connected in series thereto, wherein the switch is operative in a closed state in which current is supplied to the fusible link. It would have been obvious to one of ordinary skill in the art at the time of the invention to include a switch in the circuit to turn on and off the applied voltage to the fuse.

20. Claims 4, 8, 16, and 19 - 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iyer et al., as applied to Claims 1 – 3, 5, 13 – 15, and 17, and further in view of Wang et al.

21. Regarding Claims 4 and 16, Iyer et al. do not disclose that the material of the second material layer is tungsten silicide. Wang et al. disclose that the material of a second material layer of a fuse structure is tungsten silicide. It would have been obvious to one of ordinary skill in the art at the time of the invention to obtain a silicide layer of low resistance thereby providing efficient openings of the fuse structure.

22. Regarding Claims 8 and 19, Iyer et al. do not explicitly disclose that a data bit is represented by the open and closed state of the fuse. Wang et al. disclose (Col. 1, lines 54 – 57) that a data bit is represented by the conducting (closed) or non-conducting (open) patterns. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Iyer et al. with Wang et al. to obtain programming procedures for the fusible links.

23. Regarding Claim 20, Iyer et al. do not disclose an integrated circuit comprising active devices, wherein certain of the devices comprise a gate and the step of forming a fusible link further comprises forming a gate and fusible link region from the first material layer. Wang et al. disclose the formation of first material layer (24) (Figure 5) forming the fusible link (left side) and part of the gate (right side). It would have been obvious to one of ordinary skill in the art at

the time of the invention to combine Wang et al. with Iyer et al. to produce a working device with interconnects.

24. Regarding Claim 21, Iyer et al. do not disclose an integrated circuit comprising active devices, wherein certain of the devices are separated by isolation regions and wherein the step of forming a fusible link region further comprises forming the fusible link region over-lying an isolation region. Wang et al. disclose the presence of an isolation region (10) wherein the fusible link (200) overlies the isolation region. It would have been obvious to one of ordinary skill in the art at the time to combine Wang et al. and Iyer et al. to produce a fusible link that is isolated from adjacent devices and structure.

Conclusions

25. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
November 5, 2004

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800